

Product Summary

$V_{(BR)DSS}$	$R_{DS(ON)}$ max	I_D max $T_C = +25^\circ C$
40V	11.5m Ω @ $V_{GS} = 10V$	39A
	14.5m Ω @ $V_{GS} = 4.5V$	35A

Description

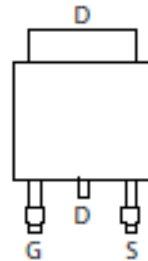
This new generation MOSFET has been designed to minimize the on-state resistance ($R_{DS(ON)}$) and yet maintain superior switching performance, making it ideal for high efficiency power management applications.

Applications

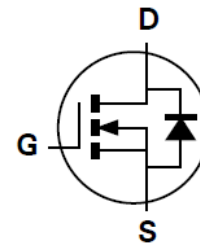
- Power management functions
- DC-DC Converters
- Backlighting



Top View



Pin Out Top View



Equivalent Circuit

Features

- Low On-Resistance
- Low Input Capacitance
- **Lead-Free Finish; RoHS Compliant (Notes 1 & 2)**
- **Halogen and Antimony Free. "Green" Device (Note 3)**
- **Qualified to AEC-Q101 Standards for High Reliability**

Mechanical Data

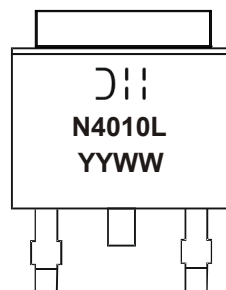
- Case: TO252-3L
- Case Material: Molded Plastic, "Green" Molding Compound.
- UL Flammability Classification Rating 94V-0
- Moisture Sensitivity: Level 1 per J-STD-020
- Terminal Connections: See Diagram
- Weight: 0.33 grams (approximate)

Ordering Information (Note 4)

Part Number	Case	Packaging
DMN4010LK3-13	TO252	2500/Tape & Reel

- Notes:
1. EU Directive 2002/95/EC (RoHS) & 2011/65/EU (RoHS 2) compliant. All applicable RoHS exemptions applied.
 2. See http://www.diodes.com/quality/lead_free.html for more information about Diodes Incorporated's definitions of Halogen- and Antimony-free, "Green" and Lead-free.
 3. Halogen- and Antimony-free "Green" products are defined as those which contain <900ppm bromine, <900ppm chlorine (<1500ppm total Br + Cl) and <1000ppm antimony compounds.
 4. For packaging details, go to our website at <http://www.diodes.com/products/packages.html>.

Marking Information



= Manufacturer's Marking
 N4010L = Product Type Marking Code
 YYWW = Date Code Marking
 YY = Last Digit of Year (ex: 13 = 2013)
 WW = Week Code (01 to 53)

Maximum Ratings (@ $T_A = +25^\circ\text{C}$, unless otherwise specified.)

Characteristic			Symbol	Value	Units
Drain-Source Voltage			V_{DSS}	40	V
Gate-Source Voltage			V_{GSS}	± 20	V
Continuous Drain Current (Note 6) $V_{GS} = 10\text{V}$	Steady State	$T_C = +25^\circ\text{C}$ $T_C = +70^\circ\text{C}$	I_D	39 31	A
	Steady State	$T_A = +25^\circ\text{C}$ $T_A = +70^\circ\text{C}$	I_D	11.9 9.5	A
Maximum Body Diode Forward Current (Note 6)			I_S	2	A
Pulsed Drain Current (10 μs pulse, Duty cycle = 1%)			I_{DM}	80	A
Avalanche Current (Notes 7) $L = 0.1\text{mH}$			I_{AS}	27	A
Avalanche Energy (Notes 7) $L = 0.1\text{mH}$			E_{AS}	37	mJ

Thermal Characteristics (@ $T_A = +25^\circ\text{C}$, unless otherwise specified.)

Characteristic		Symbol	Value	Units
Total Power Dissipation (Note 5)		P_D	1.6	W
Thermal Resistance, Junction to Ambient (Note 5)	Steady state	$R_{\theta JA}$	78	$^\circ\text{C/W}$
	$t < 10\text{s}$		31	
Total Power Dissipation (Note 6)		P_D	2.4	W
Thermal Resistance, Junction to Ambient (Note 6)	Steady state	$R_{\theta JA}$	51	$^\circ\text{C/W}$
	$t < 10\text{s}$		21	
Thermal Resistance, Junction to Case (Note 6)		$R_{\theta JC}$	4.7	
Operating and Storage Temperature Range		T_J, T_{STG}	-55 to +150	$^\circ\text{C}$

Electrical Characteristics (@ $T_A = +25^\circ\text{C}$, unless otherwise specified.)

Characteristic	Symbol	Min	Typ	Max	Unit	Test Condition
OFF CHARACTERISTICS (Note 8)						
Drain-Source Breakdown Voltage	BV_{DSS}	40	—	—	V	$V_{GS} = 0\text{V}, I_D = 250\mu\text{A}$
Zero Gate Voltage Drain Current $T_J = +25^\circ\text{C}$	I_{DSS}	—	—	1	μA	$V_{DS} = 32\text{V}, V_{GS} = 0\text{V}$
Gate-Source Leakage	I_{GSS}	—	—	± 100	nA	$V_{GS} = \pm 20\text{V}, V_{DS} = 0\text{V}$
ON CHARACTERISTICS (Note 8)						
Gate Threshold Voltage	$V_{GS(th)}$	1.0	—	3.0	V	$V_{DS} = V_{GS}, I_D = 250\mu\text{A}$
Static Drain-Source On-Resistance	$R_{DS(on)}$	—	8.7	11.5	m Ω	$V_{GS} = 10\text{V}, I_D = 14\text{A}$
		—	11.1	14.5		$V_{GS} = 4.5\text{V}, I_D = 11\text{A}$
Diode Forward Voltage	V_{SD}	—	0.72	—	V	$V_{GS} = 0\text{V}, I_S = 14\text{A}$
DYNAMIC CHARACTERISTICS (Note 9)						
Input Capacitance	C_{iss}	—	1810	—	pF	$V_{DS} = 20\text{V}, V_{GS} = 0\text{V},$ $f = 1.0\text{MHz}$
Output Capacitance	C_{oss}	—	135	—	pF	
Reverse Transfer Capacitance	C_{rss}	—	112	—	pF	
Gate Resistance	R_g	—	1.7	—	Ω	$V_{DS} = 0\text{V}, V_{GS} = 0\text{V}, f = 1\text{MHz}$
Total Gate Charge ($V_{GS} = 4.5\text{V}$)	Q_g	—	17	—	nC	$V_{DS} = 20\text{V},$ $I_D = 14\text{A}$
Total Gate Charge ($V_{GS} = 10\text{V}$)	Q_g	—	37	—	nC	
Gate-Source Charge	Q_{gs}	—	5.6	—	nC	
Gate-Drain Charge	Q_{gd}	—	7.1	—	nC	
Turn-On Delay Time	$t_{D(on)}$	—	5.1	—	ns	$V_{GS} = 10\text{V}, V_{DS} = 20\text{V},$ $R_G = 6\Omega, I_D = 14\text{A}$
Turn-On Rise Time	t_r	—	13	—	ns	
Turn-Off Delay Time	$t_{D(off)}$	—	36	—	ns	
Turn-Off Fall Time	t_f	—	13	—	ns	
Body Diode Reverse Recovery Time	t_{rr}	—	12.2	—	ns	$I_S = 3\text{A}, dI/dt = 100\text{A}/\mu\text{s}$
Body Diode Reverse Recovery Charge	Q_{rr}	—	5.4	—	nC	$I_S = 3\text{A}, dI/dt = 100\text{A}/\mu\text{s}$

- Notes:
- Device mounted on FR-4 substrate PC board, 2oz copper, with minimum recommended pad layout.
 - Device mounted on FR-4 substrate PC board, 2oz copper, with 1inch square copper plate.
 - I_{AS} and E_{AS} rating are based on low frequency and duty cycles to keep $T_J = 25^\circ\text{C}$
 - Short duration pulse test used to minimize self-heating effect.
 - Guaranteed by design. Not subject to product testing.

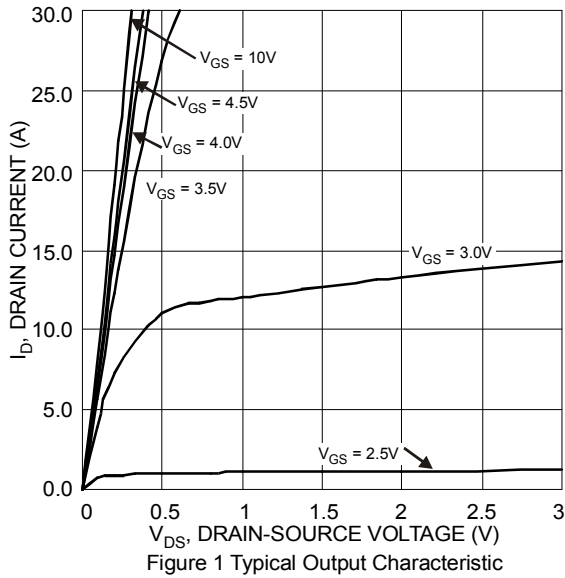


Figure 1 Typical Output Characteristic

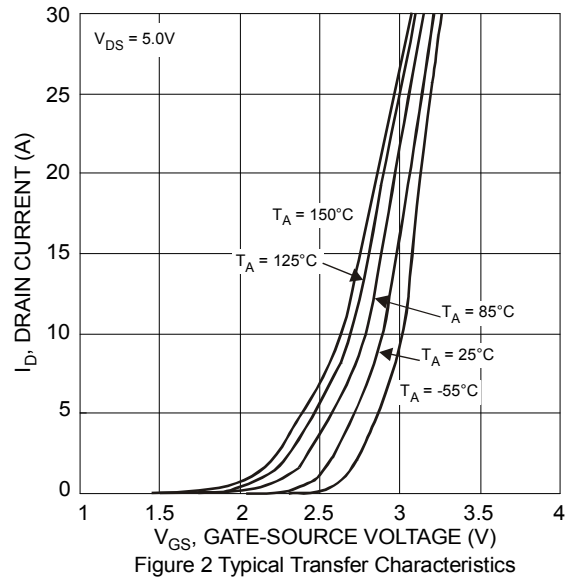


Figure 2 Typical Transfer Characteristics

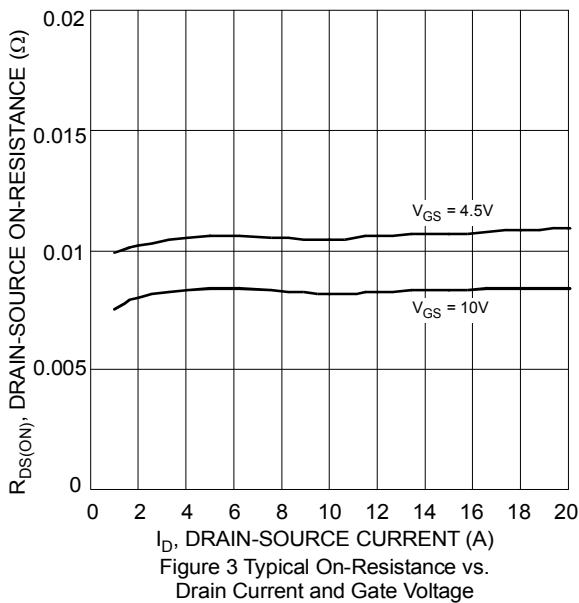


Figure 3 Typical On-Resistance vs. Drain Current and Gate Voltage

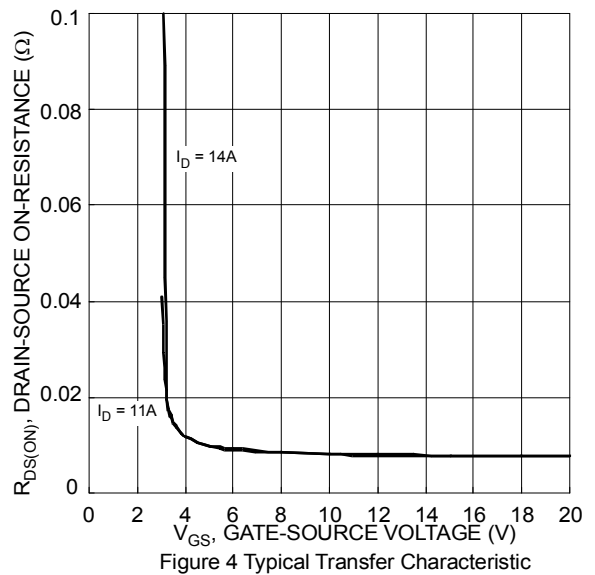


Figure 4 Typical Transfer Characteristic

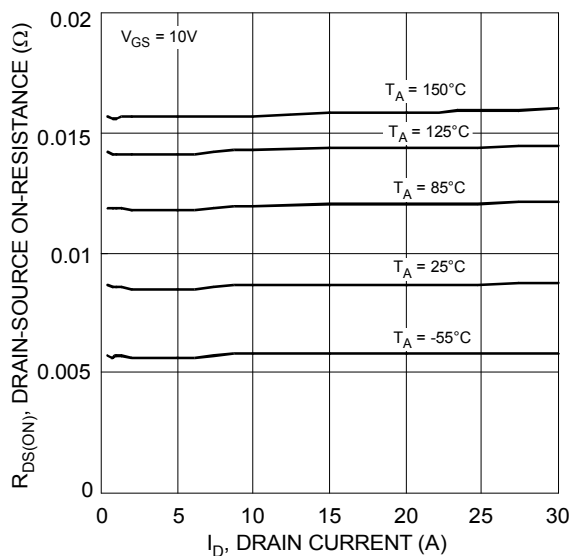


Figure 5 Typical On-Resistance vs. Drain Current and Temperature

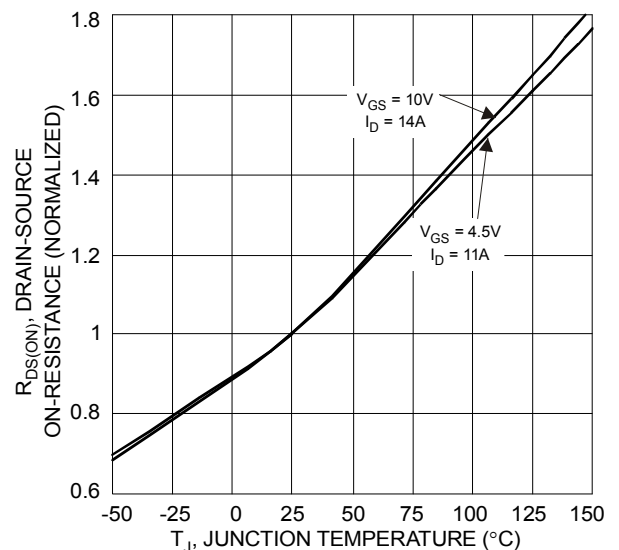


Figure 6 On-Resistance Variation with Temperature

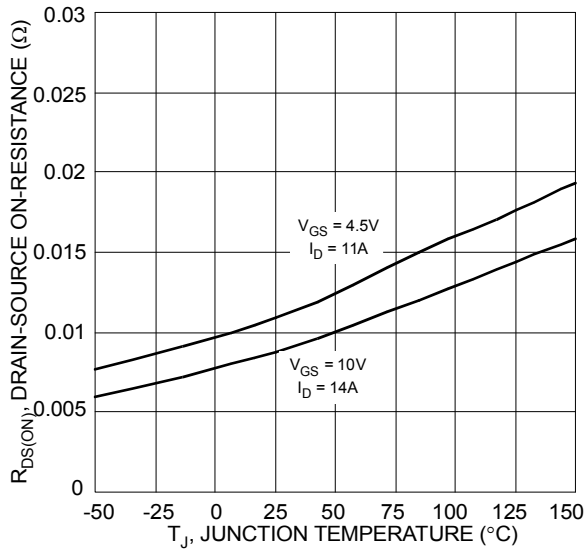


Figure 7 On-Resistance Variation with Temperature

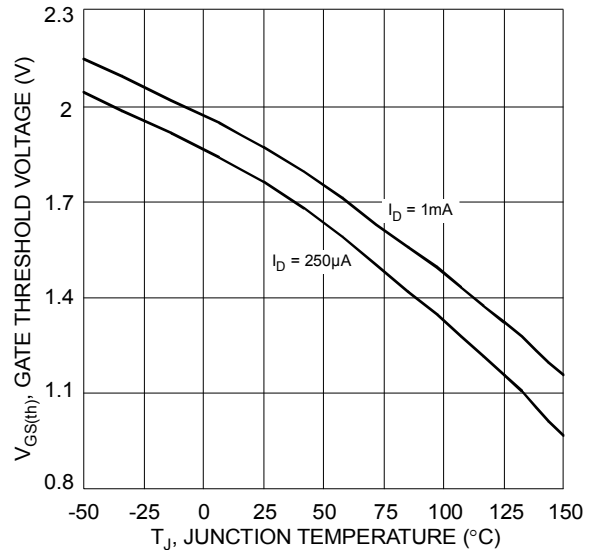


Figure 8 Gate Threshold Variation vs. Ambient Temperature

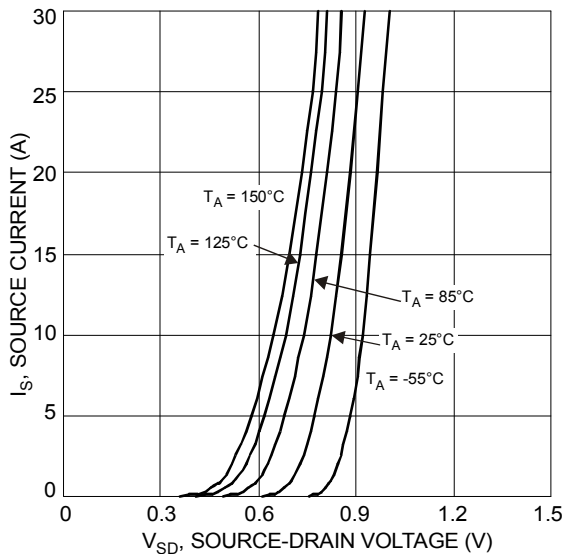


Figure 9 Diode Forward Voltage vs. Current

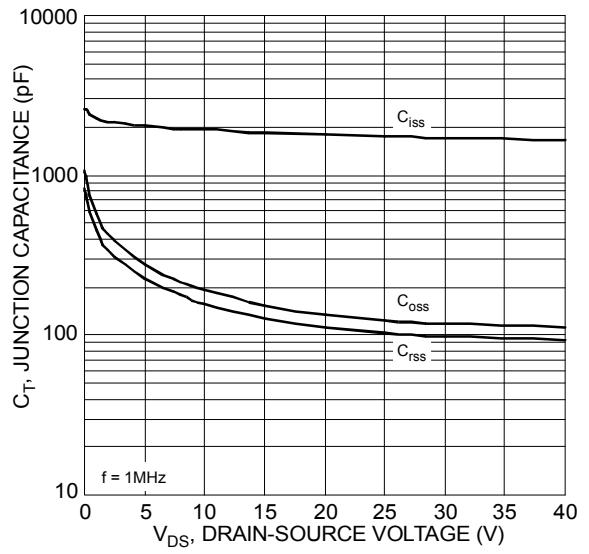


Figure 10 Typical Junction Capacitance

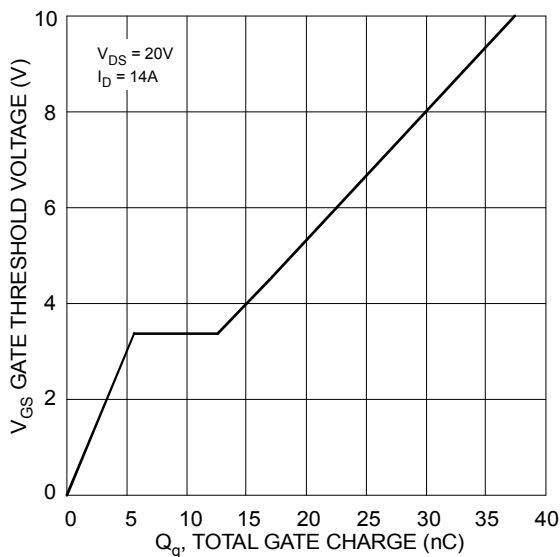


Figure 11 Gate Charge

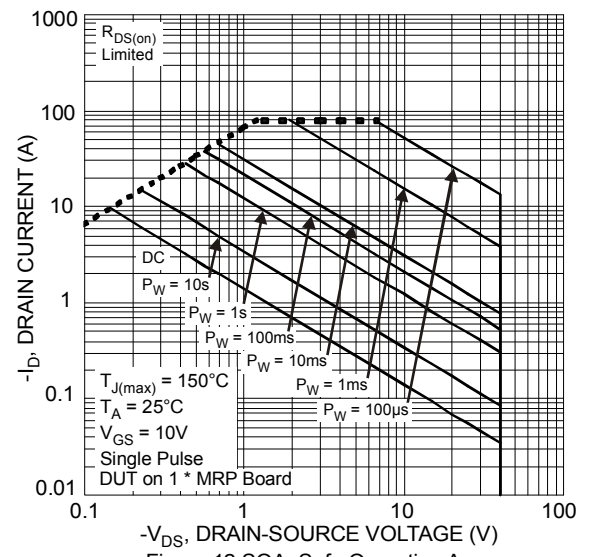


Figure 12 SOA, Safe Operation Area

NEW PRODUCT

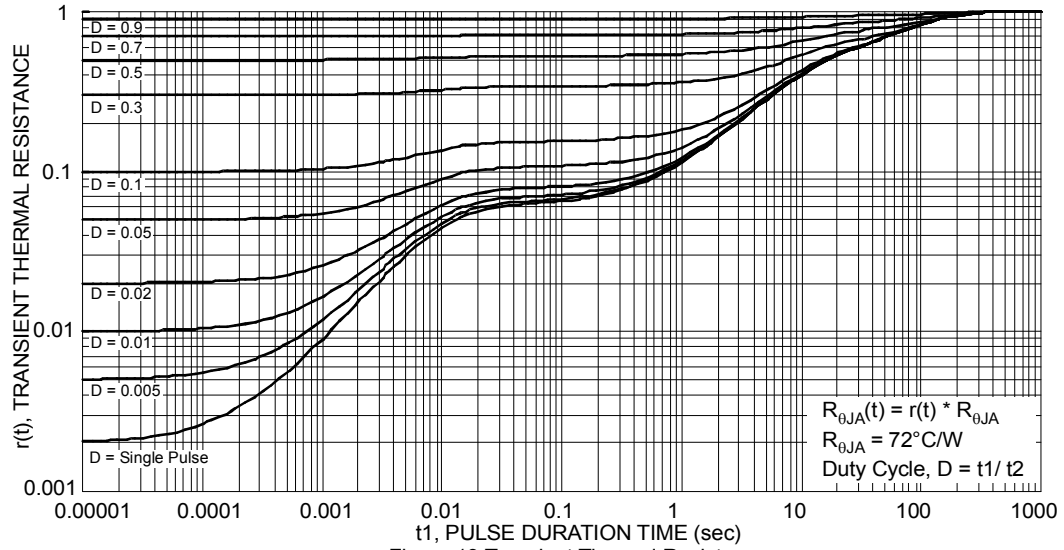
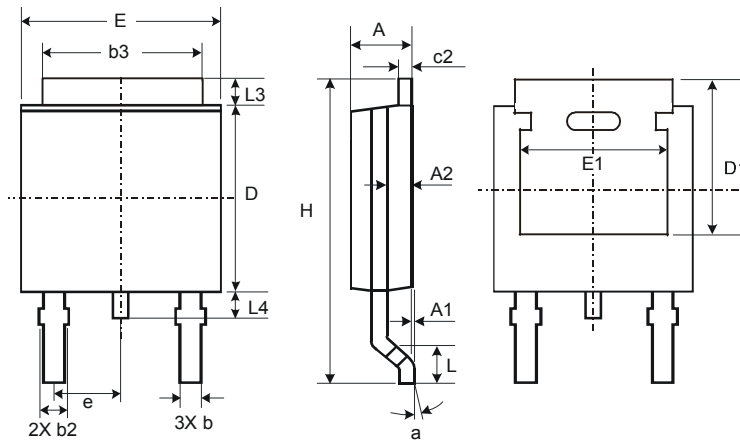


Figure 13 Transient Thermal Resistance

Package Outline Dimensions

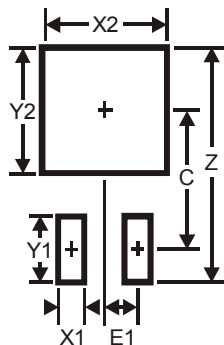
Please see AP02002 at <http://www.diodes.com/datasheets/ap02002.pdf> for latest version.



TO252			
Dim	Min	Max	Typ
A	2.19	2.39	2.29
A1	0.00	0.13	0.08
A2	0.97	1.17	1.07
b	0.64	0.88	0.783
b2	0.76	1.14	0.95
b3	5.21	5.46	5.33
c2	0.45	0.58	0.531
D	6.00	6.20	6.10
D1	5.21	-	-
e	-	-	2.286
E	6.45	6.70	6.58
E1	4.32	-	-
H	9.40	10.41	9.91
L	1.40	1.78	1.59
L3	0.88	1.27	1.08
L4	0.64	1.02	0.83
a	0°	10°	-
All Dimensions in mm			

Suggested Pad Layout

Please see AP02001 at <http://www.diodes.com/datasheets/ap02001.pdf> for the latest version.



Dimensions	Value (in mm)
Z	11.6
X1	1.5
X2	7.0
Y1	2.5
Y2	7.0
C	6.9
E1	2.3

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